M-BIT RACE DELAY ADDER AND METHOD OF OPERATION

ABSTRACT OF THE DISCLOSURE

There is disclosed an M-bit adder capable of receiving a first M-bit argument, a second M-bit argument, and a carry-in (CI) bit. The M-bit adder comprises M adder cells arranged in R rows, wherein a least significant adder cell in a first one of the rows of adder cells receives a first data bit, A_X, from the first M-bit argument and a first data bit, B_X, from the second M-bit argument, and generates a first conditional carry-out bit, $C_X(1)$, and a second conditional carry-out bit, $C_X(0)$, wherein the $C_X(1)$ bit is calculated assuming a row carry-out bit from a second row of adder cells preceding the first row is a 1 and the $C_X(0)$ bit is calculated assuming the row carry-out bit from the second row is a 0.